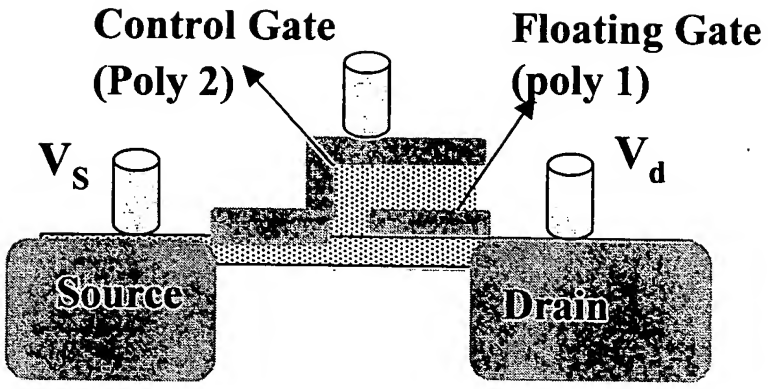


FIG 1

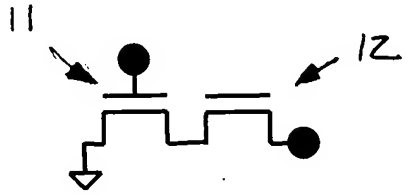


FIG 1A

SG EE	Erase	Program	Read
SG Wordline (WL)	-17V (-12V)	Vt	Vref
Bitline (BL)	Vss (5V)	12V	Vdd
Source line (SR)	Vss	Vss	Vss

FIG 1B

FIG. 2A

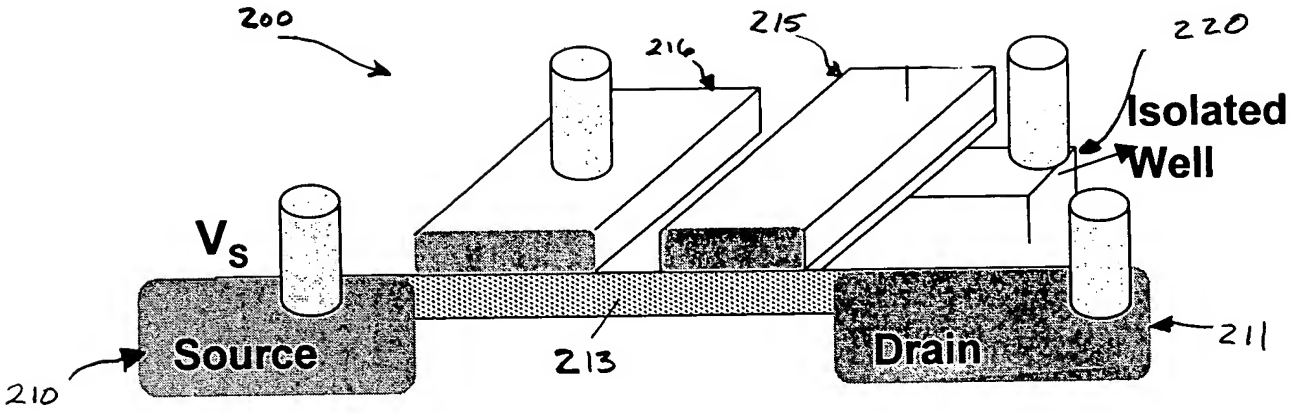
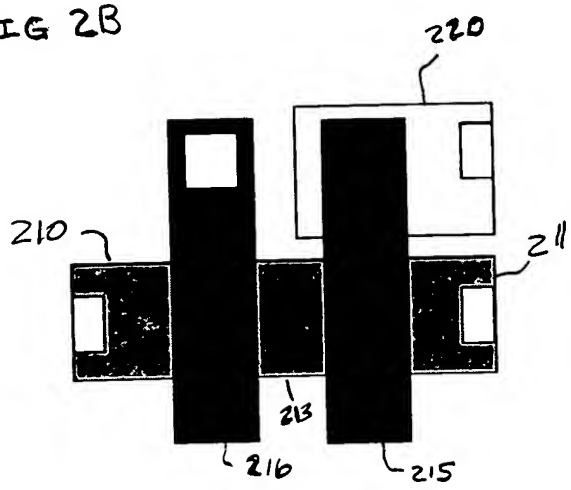

200
216
215
220
Isolated
Well
V_S
Source
213
Drain
211
210

FIG 2B


220
210
211
213
216
215

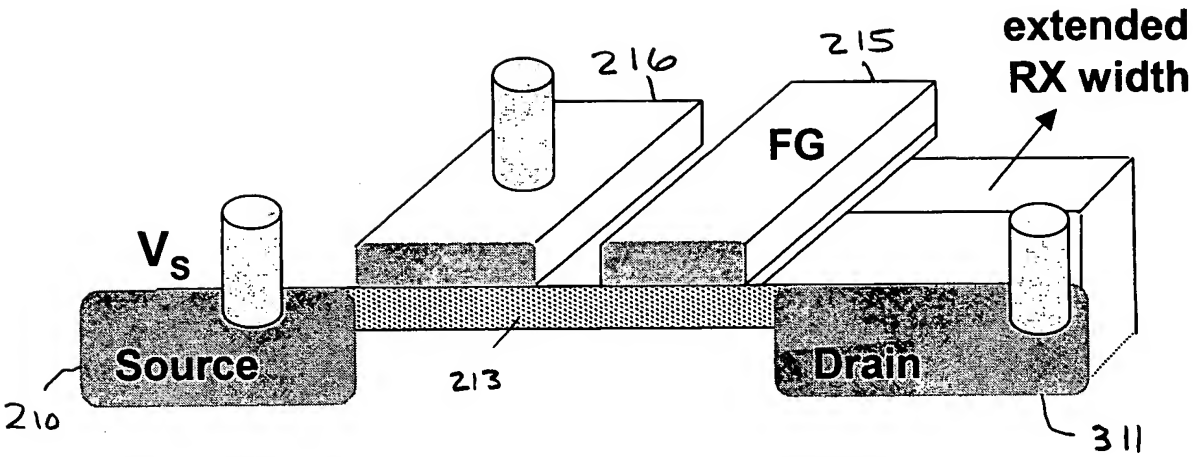

extended
RX width
216
215
FG
V_S
Source
213
Drain
210
311

FIG 3A

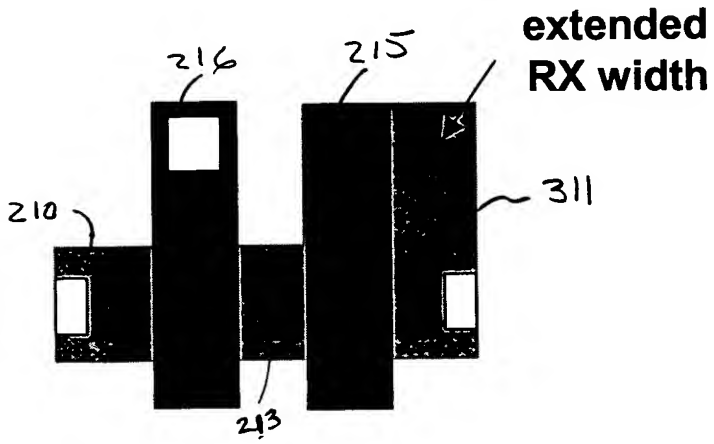

extended
RX width
216
215
311
210
213

FIG 3B

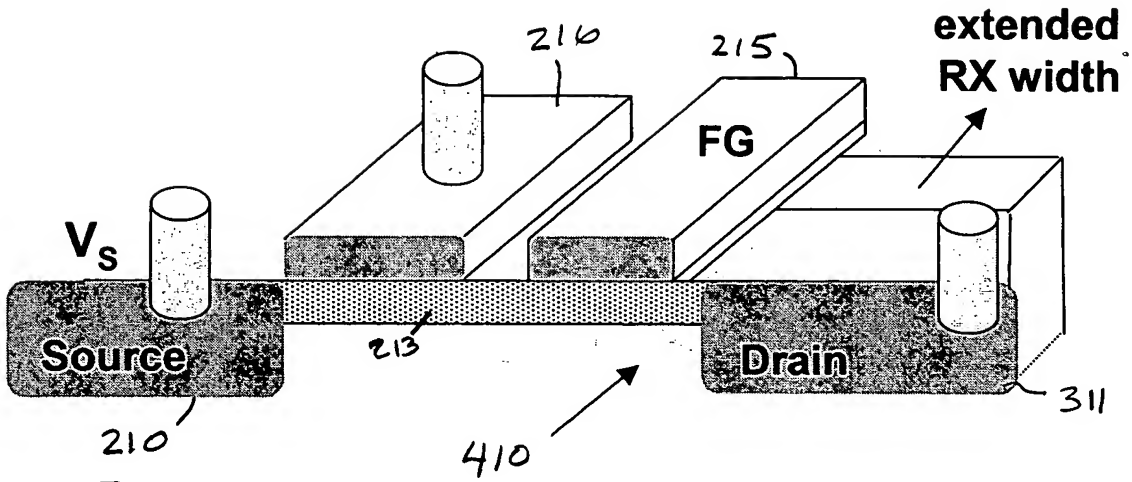

216
215
extended
RX width
FG
V_S
Source
213
Drain
311
210
410

FIG. 4A

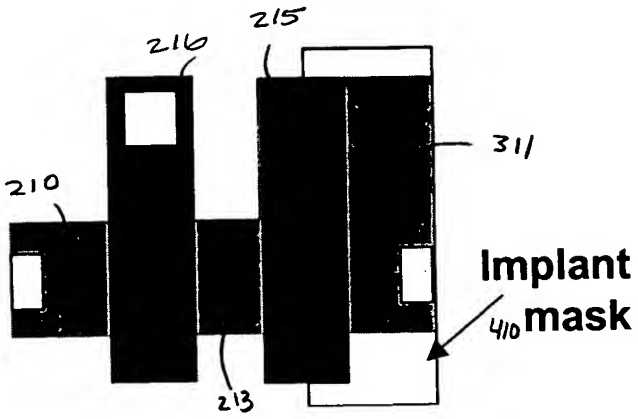

216
215
311
210
Implant
410 mask
213

FIG. 4B

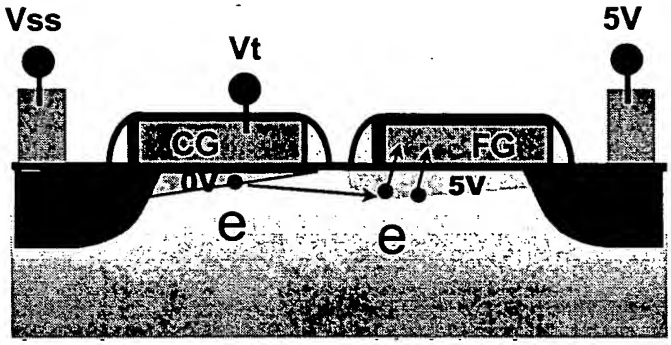
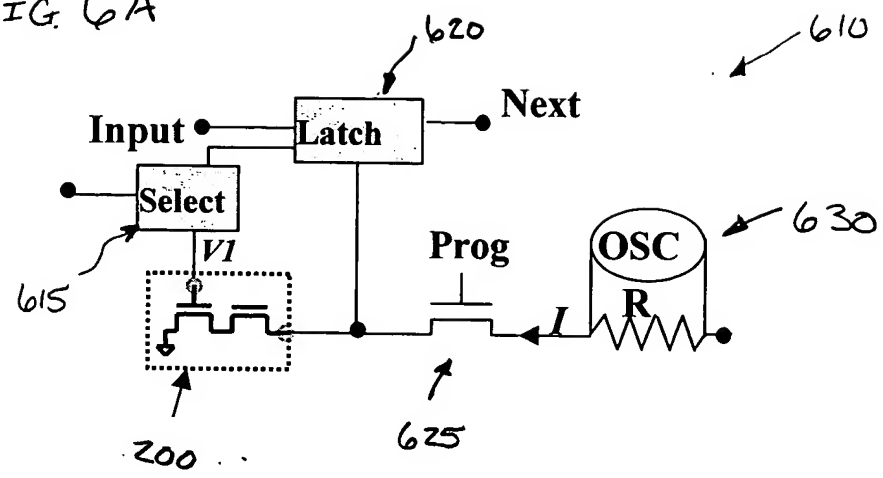


FIG 5A

NVM fuse	Erase	Program	Read
selected Wordline	-5V	Vt	Vref
BL (+ iso-well)	5V	5V	Vdd
Source	Vss	Vss	Vss

FIG 5B

FIG. 6A



NVM fuse	Erase	Program	Read
Select (WL)	-5V	Vt	Vref
Latch BL (Prog FET)	5V	5V (on)	Vdd (off)
Source	Vss	Vss	Vss

FIG. 6B

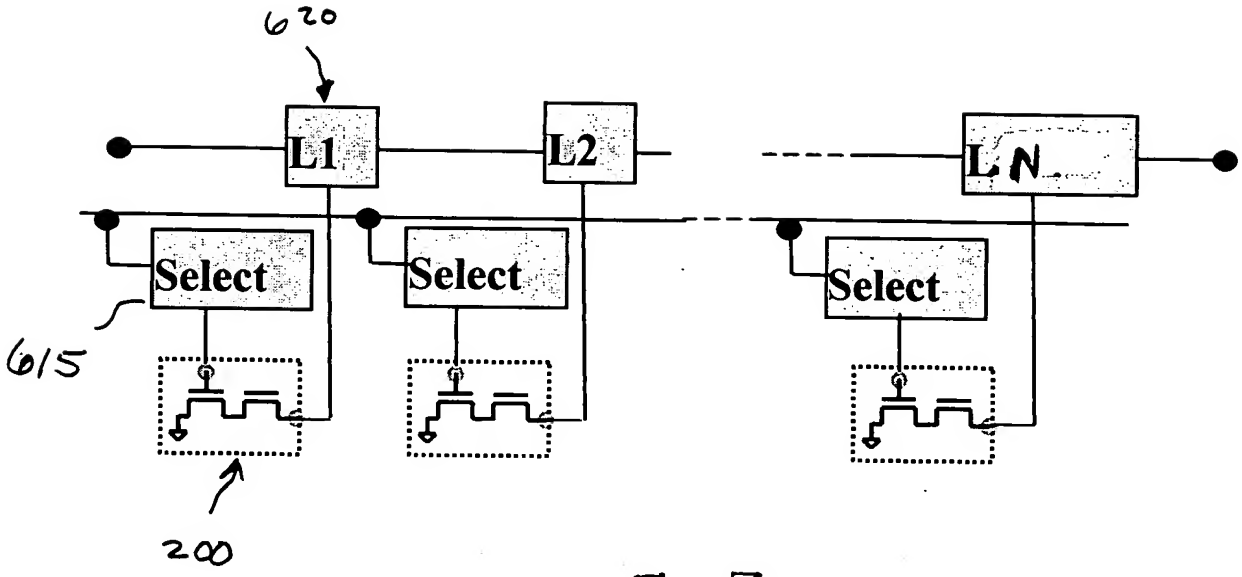


FIG. 7